FIG. 1

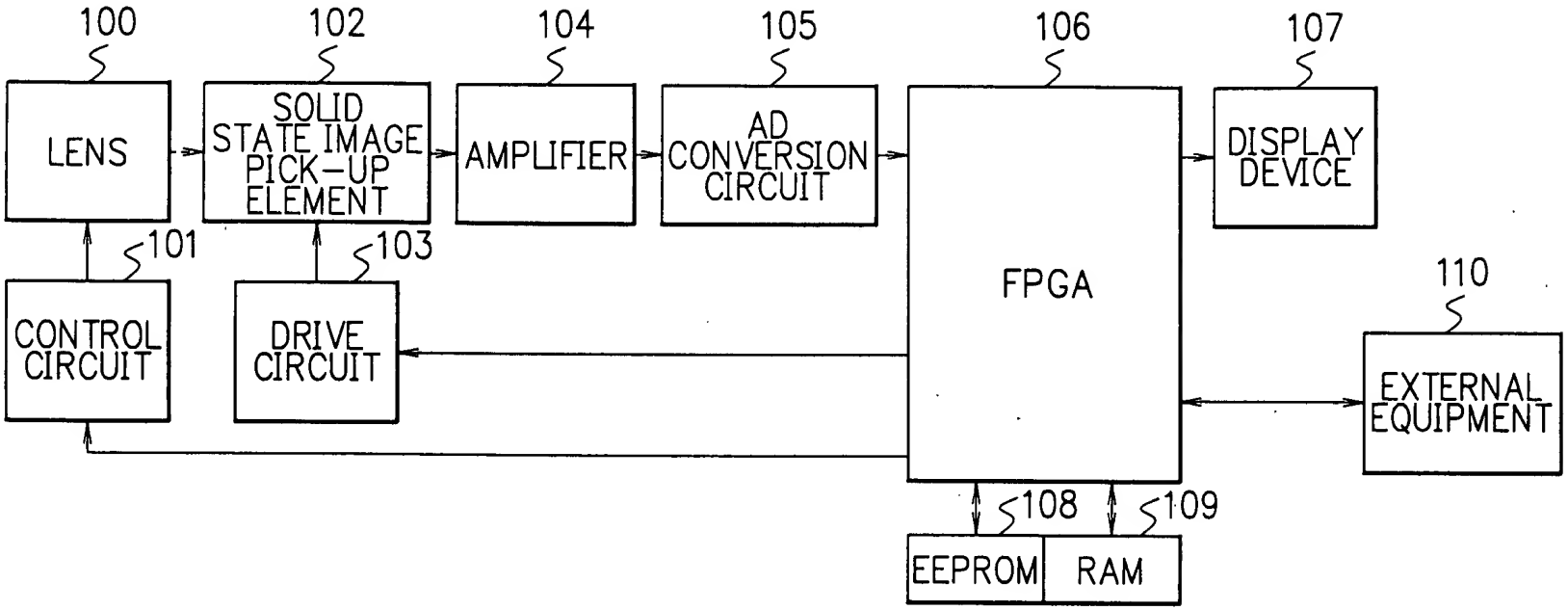


FIG. 2

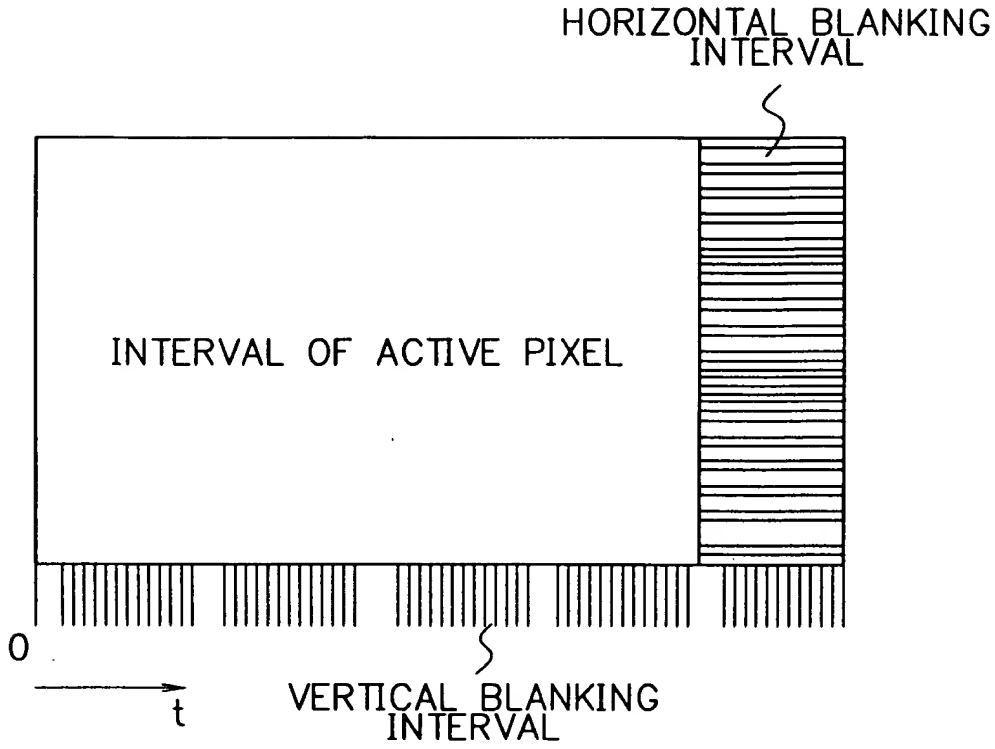

HORIZONTAL BLANKING INTERVAL
INTERVAL OF ACTIVE PIXEL
0
t
VERTICAL BLANKING INTERVAL

FIG. 3

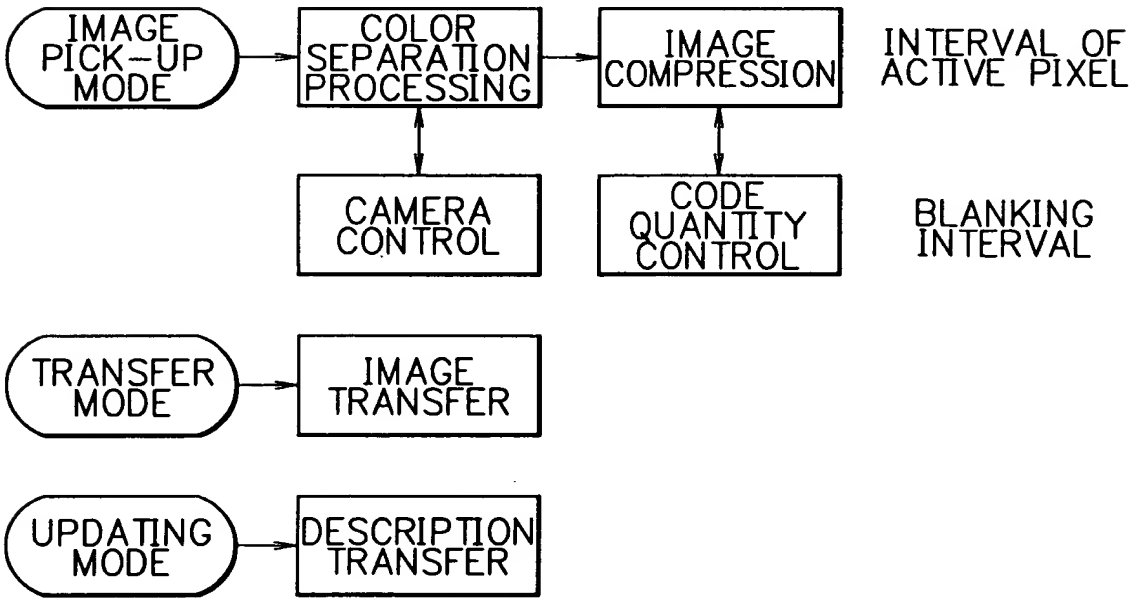


IMAGE PICK-UP MODE
COLOR SEPARATION PROCESSING
IMAGE COMPRESSION
INTERVAL OF ACTIVE PIXEL
CAMERA CONTROL
CODE QUANTITY CONTROL
BLANKING INTERVAL
TRANSFER MODE
IMAGE TRANSFER
UPDATING MODE
DESCRIPTION TRANSFER

FIG. 4

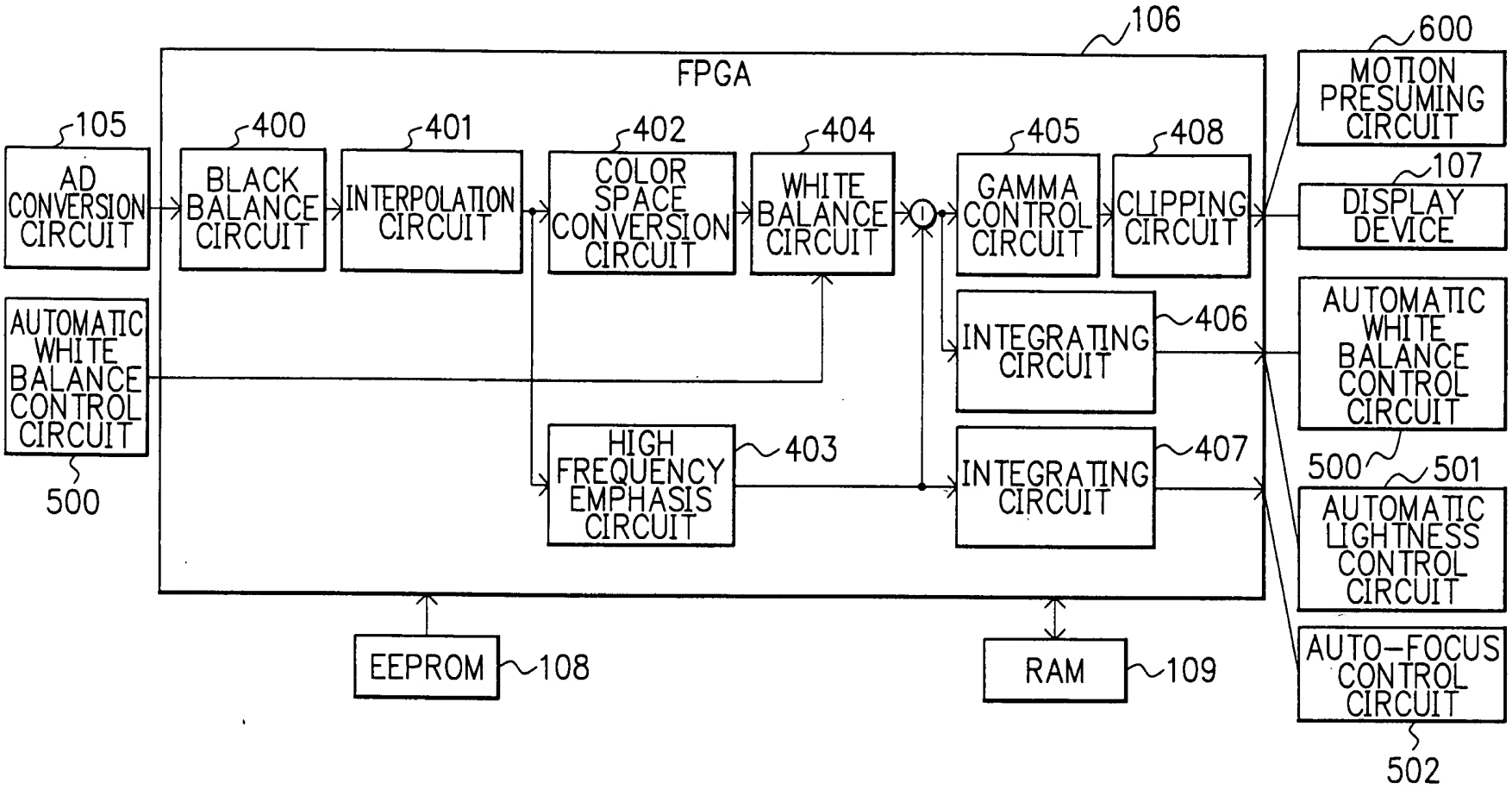

106
FPGA
105
AD CONVERSION CIRCUIT
400
BLACK BALANCE CIRCUIT
401
INTERPOLATION CIRCUIT
402
COLOR SPACE CONVERSION CIRCUIT
404
WHITE BALANCE CIRCUIT
405
GAMMA CONTROL CIRCUIT
408
CLIPPING CIRCUIT
600
MOTION PRESUMING CIRCUIT
107
DISPLAY DEVICE
AUTOMATIC WHITE BALANCE CONTROL CIRCUIT
500
406
INTEGRATING CIRCUIT
AUTOMATIC WHITE BALANCE CONTROL CIRCUIT
HIGH FREQUENCY EMPHASIS CIRCUIT
403
407
INTEGRATING CIRCUIT
500
501
AUTOMATIC LIGHTNESS CONTROL CIRCUIT
EEPROM
108
RAM
109
AUTO-FOCUS CONTROL CIRCUIT
502

FIG. 5

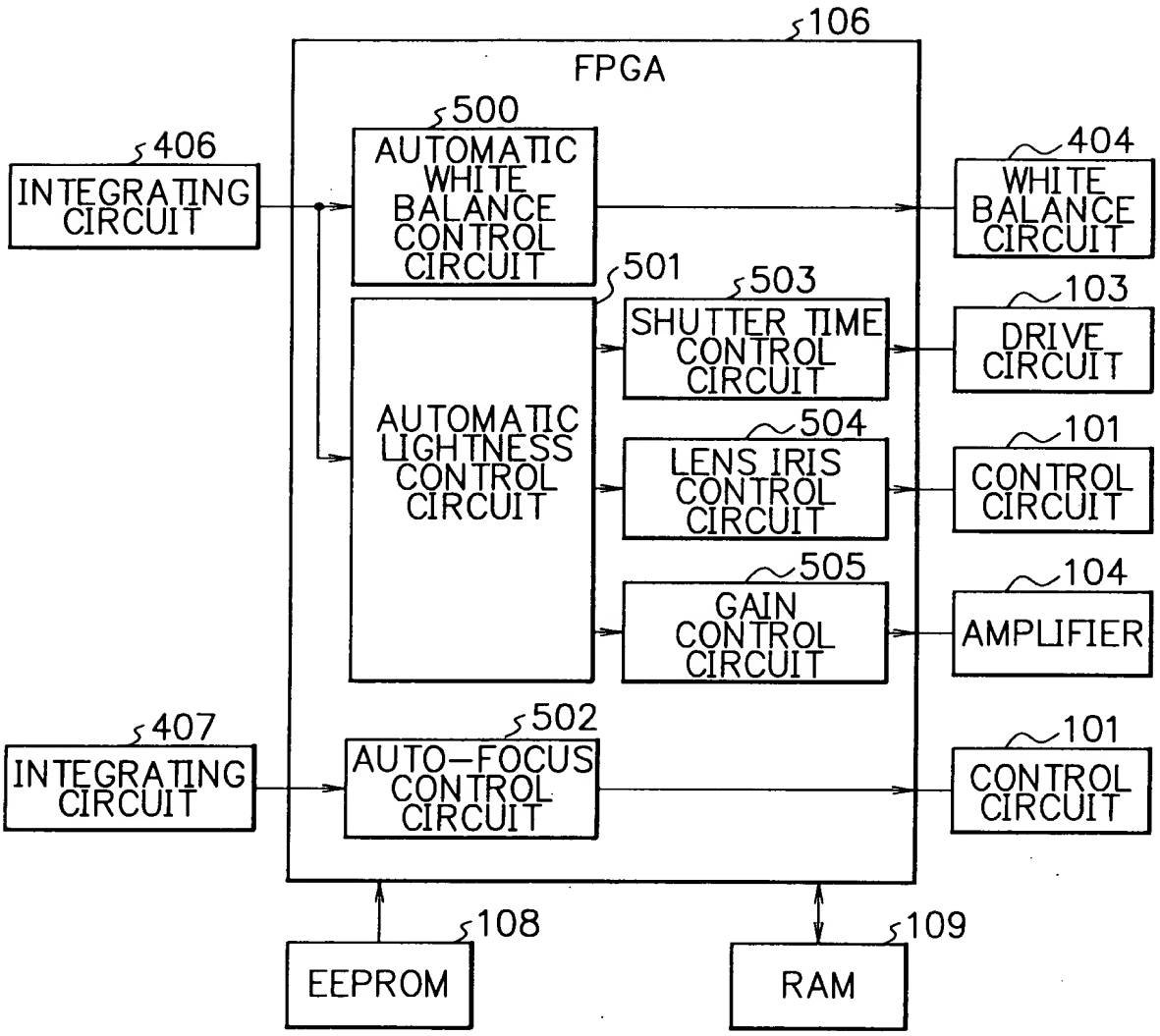

106
FPGA
500
AUTOMATIC WHITE BALANCE CONTROL CIRCUIT
406
INTEGRATING CIRCUIT
404
WHITE BALANCE CIRCUIT
501
503
SHUTTER TIME CONTROL CIRCUIT
103
DRIVE CIRCUIT
AUTOMATIC LIGHTNESS CONTROL CIRCUIT
504
LENS IRIS CONTROL CIRCUIT
101
CONTROL CIRCUIT
505
GAIN CONTROL CIRCUIT
104
AMPLIFIER
407
INTEGRATING CIRCUIT
502
AUTO-FOCUS CONTROL CIRCUIT
101
CONTROL CIRCUIT
108
EEPROM
109
RAM

FIG. 6

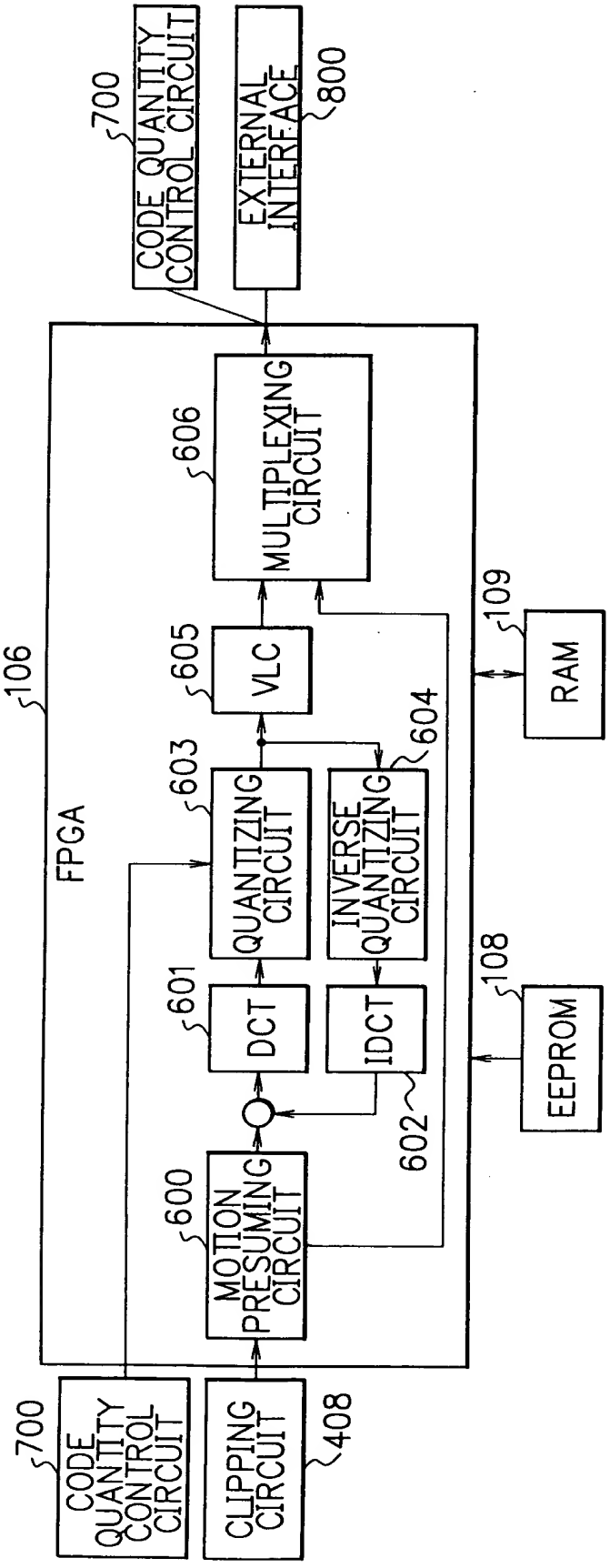

CODE QUANTITY CONTROL CIRCUIT
700
EXTERNAL INTERFACE
800
FPGA
106
MULTIPLEXING CIRCUIT
606
VLC
605
QUANTIZING CIRCUIT
603
INVERSE QUANTIZING CIRCUIT
604
RAM
109
DCT
601
IDCT
602
MOTION PRESUMING CIRCUIT
600
EEPROM
108
CODE QUANTITY CONTROL CIRCUIT
700
CLIPPING CIRCUIT
408

FIG. 7

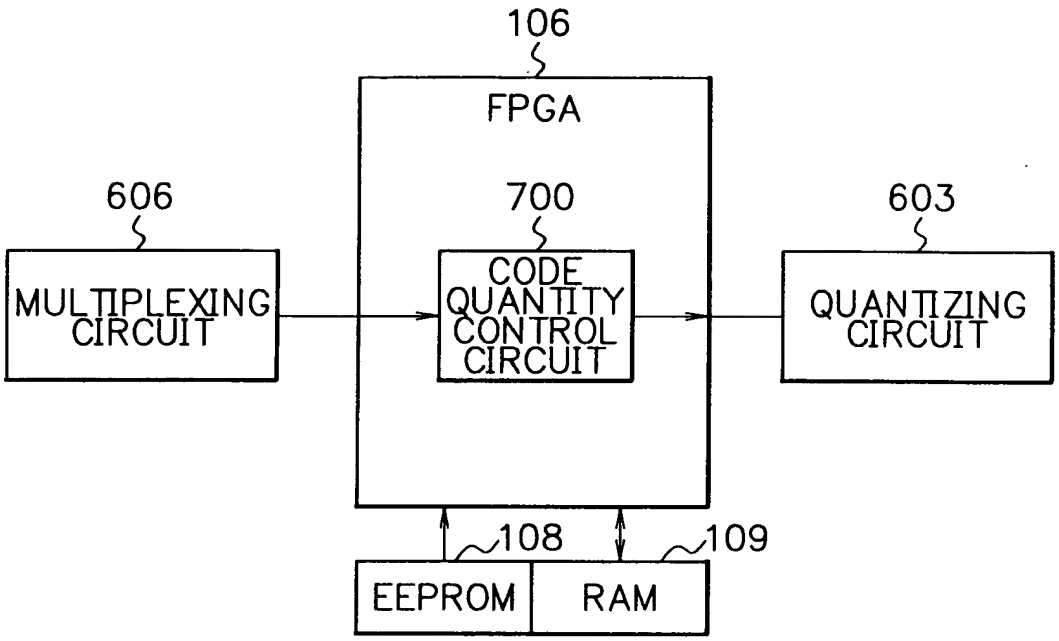

106
FPGA
606
MULTIPLEXING CIRCUIT
700
CODE QUANTITY CONTROL CIRCUIT
603
QUANTIZING CIRCUIT
108
109
EEPROM
RAM

FIG. 8

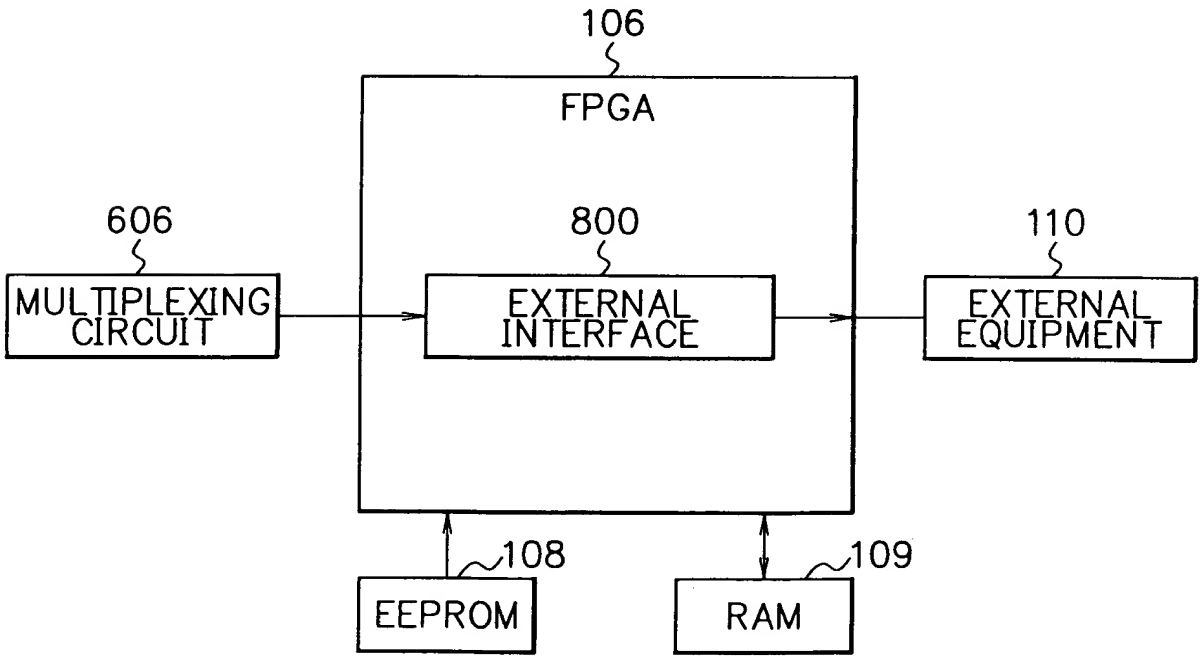
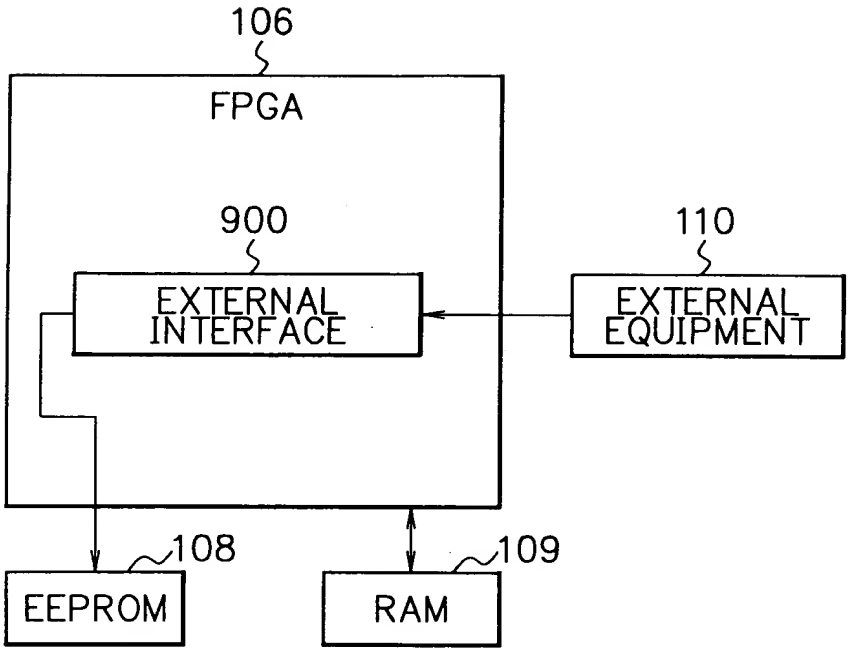

106
FPGA
606
MULTIPLEXING CIRCUIT
800
EXTERNAL INTERFACE
110
EXTERNAL EQUIPMENT
108
109
EEPROM
RAM

FIG. 9


106
FPGA
900
EXTERNAL INTERFACE
110
EXTERNAL EQUIPMENT
108
EEPROM
109
RAM